Intel® I225/I226 Reference Schematic
February 2024 Rev2.8
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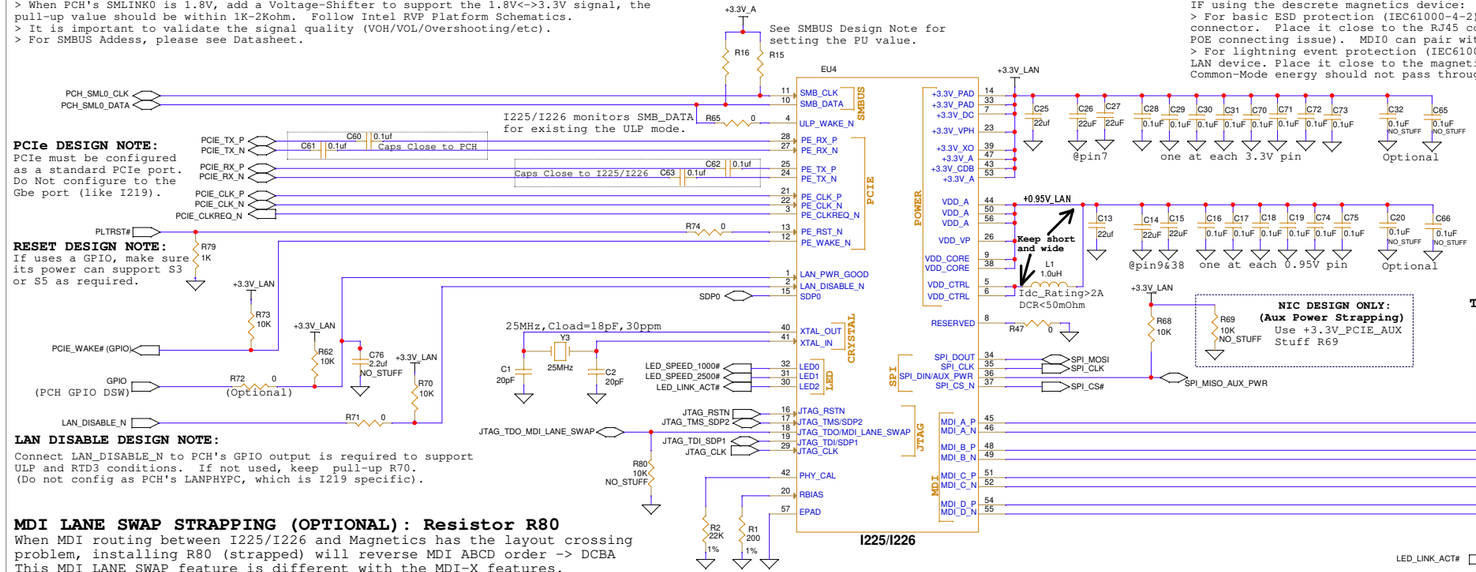
SMBUS DESIGN NOTE:
> For non-vPRO or standard PCIe device: SMBUS is not required (10K pull-ups to +3.3V_LAN).
> For vPRO platforms: I225/I226 SMBUS must connect to PCH's SMLINK0.
> The pull-up power rail should be same with PCH's SMLINK0 power rail.
> I225/I226 SMBUS speed default is 1MHz
> When PCH's SMLINK0 is 3.3V, the pull-up should be 499ohm.
> When PCH's SMLINK0 is 1.8V, add a Voltage-Shifter to support the 1.8V<->3.3V signal, the pull-up value should be within 1K-2Kohm. Follow Intel RVP Platform Schematics.
> It is important to validate the signal quality (VOH/VOL/Overshooting/etc).
> For SMBUS Address, please see Datasheet.



PCIe DESIGN NOTE:
PCIe must be configured as a standard PCIe port. Do Not configure to the Gbe port (like I219).

RESET DESIGN NOTE:
If uses a GPIO, make sure its power can support S3 or S5 as required.

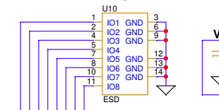
LAN DISABLE DESIGN NOTE:
Connect LAN_DISABLE_N to PCH's GPIO output is required to support ULP and RTD3 conditions. If not used, keep pull-up R70. (Do not config as PCH's LANPHYPC, which is I219 specific).

ESD/TVS DESIGN NOTE:
* This schematic is using the integrated magnetics RJ45 connector. Place ESD devices close to the RJ45 connector. MDI0 and MDI1 paring on a same ESD is ok (no PoE connecting issue).
IF using the descrete magnetics device:
> For basic ESD protection (IEC61000-4-2), place the ESD devices between the magnetics device and the RJ45 connector. Place it close to the RJ45 connector. Do not pair MDI0 and MDI1 on a same ESD device (avoid LAN POE connecting issue). MDI0 can pair with either MDI2 or MDI3 on a same ESD.
> For lightning event protection (IEC61000-4-5), place the ESD devices between the magnetics device and the LAN device. Place it close to the magnetics device. MDI0 and MDI1 paring on a same ESD is ok (because PoE Common-Mode energy should not pass through the magnetics device).

VCT DESIGN NOTE:
The Magnetic Core Center-Tap pins must have decoupling capacitors (either integrated insdie the Magnetics part or external caps). Double check Magnetics Datasheet.
> If the magnetics already have 4x0.1uF integrated caps (like this connector). We do not need any external caps. Suggest an empty 0.1uF cap as the place holder.
> If the magnetics part does NOT have any integrated caps, we must add 4x0.1uF external caps (one at each Vct pin). Tie all 4x0.1uF together might improve EMI performance.

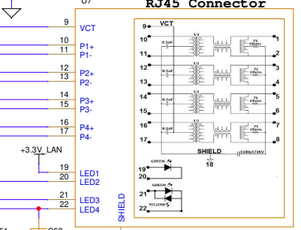
NIC DESIGN ONLY: (Aux Power Strapping)
Use +3.3V_PCIE_AUX
Stuff R69

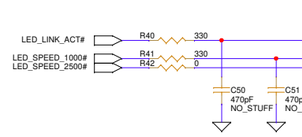
TVS Device (optional)



MAGNETICS DESIGN NOTE:
The Common-Mode Chokes of Magnetics are referred to be on the Cable Side, but not required.

Integrated Magnetics RJ45 Connector



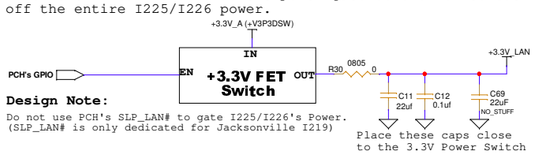


MDI LANE SWAP STRAPPING (OPTIONAL): Resistor R80
When MDI routing between I225/I226 and Magnetics has the layout crossing problem, installing R80 (strapped) will reverse MDI ABCD order -> DCBA
This MDI LANE SWAP feature is different with the MDI-X features.
See I225/I226 Design Consideration and Datasheet for more details.

To Support Device D3: Foxville I225/I226 MUST have its own RESET#, CLKREQ#, WAKE#, and Power Control/Enable.

CRYSTAL DESIGN NOTE:
> Keep Crystal circuit close to I225/I226 as much as possible.
> Always do Crystal validation for production quality.
> I225/I226 supports Cload=18pF Crystals, using formula Cload=[(C1*C2)/(C1+C2)] + Cstray. (Cstray is varied. It is based on specific board stack-up, silicon pads, traces, etc.)
If Cstray=9pF, then select C1=C2= 18pF
If Cstray=8pF, then select C1=C2= 20pF <-suggest this value as default.
If Cstray=7pF, then select C1=C2= 22pF
> Please measure Crystal PPM frequency accuracy during electrical validation.
> Intel validated I225/I226 with the Cload=18pF Crystals. For other values, please consult with Intel and Crystal Part Vendor for specific requirements.

POWER DESIGN NOTE: (Mandatory)
> +3.3V_LAN should always have power during all networking conditions (for supporting S0, Sx, DeepSx states, WOL, etc.)
> PCH's GPIO can be used as the power gate controller to cut off the entire I225/I226 power.

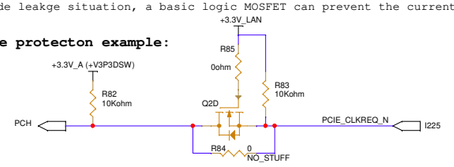


Design Note:
Do not use PCH's SLP_LAN# to gate I225/I226's Power. (SLP_LAN# is only dedicated for Jacksonville I219)

POTENTIAL LEAKAGE CURRENT (I225 ONLY)
*NOTE: I226 does not have this potential leakage current.

If I225 power is connecting directly to the +3.3V_A/+V3P3DSW power rail (the Power FET Switch is not used), we should not have leakage currents.
If the Power FET Switch is used to turns off I225 power in DeepSx/Sx/SOix, the following pins might have potential leakage issue:
* Pin 3: PE_CLKREQ_N
* Pin 4: ULP_WAKE_N
* Pin 10/11: SMBUS DATA/CLK
* Pin 12: PE_WAKE_N
To avoide leakge situation, a basic logic MOSFET can prevent the current path.

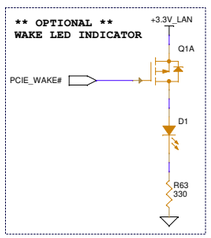
Leakage protecton example:



The Voltage-Level Shifter can also prevent the leakage current.
Always check the leakage current issues for production quality.

LED DESIGN NOTE:
There is no specific industrial standard for Ethernet LEDs.
This schematic just shows the most common SPEED LED configuration:
Highest Speed = Green
2nd Highest Speed = Yellow
All other lower Speeds = OFF
No Cable/Link = OFF
All LED pins are set active low. See Datasheet for additional info.
Adjust R40/R41/R42 value for LED brightness.

**** OPTIONAL ** WAKE LED INDICATOR**

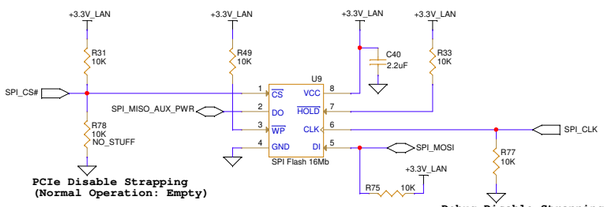


SPEED LED

SPEED	COLOR
2500 Mbps	GREEN
1000 Mbps	YELLOW
100/10 Mbps	OFF
NO LINK	OFF

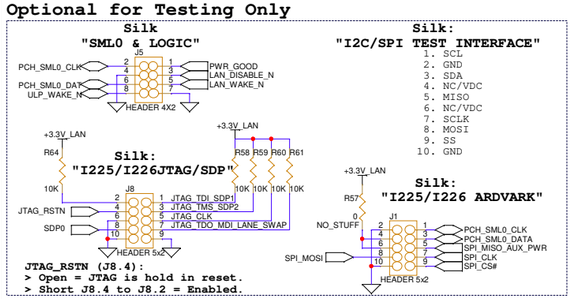
LINK/ACTIVE LED

CONDITION	COLOR
LINK-UP	SOLID GREEN
TRAFFIC	BLINKING GREEN
LINK-DOWN	OFF



SPI FLASH DESIGN NOTE:
> 8Mb SPI Flash can be used when Option-Rom is not needed.
> 16Mb SPI Flash is required for supporting Option-ROM (PXE/Etc).

Optional for Testing Only



REVISION HISTORY

REV	NOTES	DATE
0.9	1st release	July/2018
2.0	FINAL RELEASE Add MDI Lane Swap feature & leakage info. Update design notes.	October, 2020
2.1	PWR_GOOD Connection. Update design notes.	February, 2021
2.5	Add I226	November, 2021
2.6	Update design notes.	February, 2022
2.7	Remove Optional Security Trap. Update design notes.	March, 2022
2.8	Add a capacitor for LAN_PWR_Good. Add Mandatory for 3V3 Mosfet.	February, 2024

NOTE: This is a typical design. Please see the I225/I226 Design Checklist for more details requirements.